

Application No. 10/604,323

Amendment dated July 22, 2005

Amendment made in response to Office Action dated April 22, 2005

Amendments to Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A barrier stack comprising:
a first sub-barrier layer, the first sub-barrier layer comprises a first sub-barrier conductive barrier material, the first sub-barrier layer includes grain boundaries layer; and
a second sub-barrier layer disposed above the first sub-barrier layer, the second sub-barrier layer comprises a second sub-barrier conductive barrier material, the second sub-barrier layer includes grain boundaries; and
passivating elements are provided to passivate grain boundaries on an upper surface of the first sub-barrier layer ~~a second barrier layer above the first barrier layer, the second barrier layer comprises a conductive oxide to enhance the barrier properties of the barrier stack.~~
2. (original) The barrier stack of claim 1 serves as a barrier for capacitor over plug structure of a memory cell.
3. (original) The barrier stack of claim 2 wherein the capacitor over plug structure includes a plug having a step over an ILD layer.
4. (currently amended) The barrier stack of claim ~~2~~ 1 serves as a barrier for capacitor over plug structure of further comprises a plurality of memory cells arranged in a series architecture.
5. (original) The barrier stack of claim 4 wherein the capacitor over plug structure includes a plug having a step over an ILD layer.

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6. (original) The barrier stack of claim 1 serves as a barrier for capacitor over plug structure of a ferroelectric memory cell.
7. (original) The barrier stack of claim 6 wherein the capacitor over plug structure includes a plug having a step over an ILD layer.
8. (currently amended) The barrier stack of claim 6 1 serves as a barrier for capacitor over plug structure of ~~farther comprises~~ a plurality of ferroelectric memory cells arranged in a series architecture.
9. (original) The barrier stack of claim 8 wherein the capacitor over plug structure includes a plug having a step over an ILD layer.
10. (cancelled)
11. (cancelled)
12. (cancelled)
13. (cancelled)
14. (cancelled)
15. (cancelled)
16. (cancelled)

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17. (cancelled)

18. (currently amended) The barrier stack of claim 1 wherein ~~an RTO is performed after the first barrier layer is formed and before the second barrier layer is formed~~ the passivating elements comprises oxygen.

19. (currently amended) The barrier stack of claim 18 wherein:
the first sub-barrier material ~~barrier layers~~ comprises Ir, Ru, Rh, Pd, Hf or a combination thereof; and
the second sub-barrier material comprises Ir, Ru, Rh, Pd, Hf, a conductive oxide or a combination thereof.

20. (currently amended) The barrier stack of claim 19 wherein the ~~second barrier layer comprises oxides of Ir, Ru, Rh, Pd, Hf or a combination thereof~~ grain boundaries of the first and second sub-barrier layers are mismatched.

21. (currently amended) The barrier stack of claim ~~18~~ 19 wherein the ~~second barrier layer comprises oxides of Ir, Ru, Rh, Pd, Hf or a combination thereof~~ grain boundaries of the first and second sub-barrier layers are mismatched.

22. (cancelled)

23. (new) The barrier stack of claim 1 wherein:
the first sub-barrier material comprises Ir, Ru, Rh, Pd, Hf or a combination thereof; and
the second sub-barrier material comprises Ir, Ru, Rh, Pd, Hf, a conductive oxide or a combination thereof.

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24. (new) The barrier stack of claim 23 wherein the grain boundaries of the first and second sub-barrier layers are mismatched.
25. (new) The barrier stack of claim 1 wherein the grain boundaries of the first and second sub-barrier layers are mismatched.
26. (new) The barrier stack of claim 23 wherein the passivating elements comprises a size greater than the grain boundaries of the first sub-barrier layer.
27. (new) The barrier stack of claim 26 wherein:
the first sub-barrier material comprises Ir, Ru, Rh, Pd, Hf or a combination thereof; and
the second sub-barrier material comprises Ir, Ru, Rh, Pd, Hf, a conductive oxide or a combination thereof.
28. (new) The barrier stack of claim 27 wherein the grain boundaries of the first and second sub-barrier layers are mismatched.
29. (new) The barrier stack of claim 26 wherein the grain boundaries of the first and second sub-barrier layers are mismatched.
30. (new) The barrier stack of claim 1 further comprises an upper barrier layer disposed above the second sub-barrier layer, the upper barrier layer comprises a conductive oxide.
- 31 (new) The barrier stack of claim 30 wherein the passivating elements comprises a size greater than the grain boundaries of the first sub-barrier layer.

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32. (new) The barrier stack of claim 30 wherein the passivating elements comprises oxygen.

33. (new) The barrier stack of claim 30 wherein:
the first sub-barrier material comprises Ir, Ru, Rh, Pd, Hf or a combination thereof; and
the second sub-barrier material comprises Ir, Ru, Rh, Pd, Hf, a conductive oxide or a combination thereof.

34. (new) The barrier stack of claim 30 wherein the grain boundaries of the first and second sub-barrier layers are mismatched.

35. (new) The barrier stack of claim 30 wherein the grain boundaries of the upper barrier and second sub-barrier layers are mismatched.

36. (new) A barrier stack comprising:
a first sub-barrier layer, the first sub-barrier layer comprises a first sub-barrier conductive barrier material, the first sub-barrier layer includes grain boundaries;
a second sub-barrier layer disposed above the first sub-barrier layer, the second sub-barrier layer comprises a second sub-barrier conductive barrier material, the second sub-barrier layer includes grain boundaries; and
passivating elements are provided to passivate grain boundaries on an upper surface of the first sub-barrier layer, wherein the passivating elements comprises a size greater than the grain boundaries of the first sub-barrier layer.

37. (new) A barrier stack comprising:
a first sub-barrier layer, the first sub-barrier layer comprises a first sub-barrier conductive barrier material, the first sub-barrier layer includes grain boundaries;

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a second sub-barrier layer disposed above the first sub-barrier layer, the second sub-barrier layer comprises a second sub-barrier conductive barrier material, the second sub-barrier layer includes grain boundaries;

wherein grain boundaries of the first and second sub-barrier layers are mismatched; and

passivating elements are provided to passivate grain boundaries on an upper surface of the first sub-barrier layer.